
EXHIBIT C

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571-272-7822

Paper 9
Date: November 8, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WOLFSPEED, INC.,
Petitioner,

v.

THE TRUSTEES OF PURDUE UNIVERSITY,
Patent Owner.

IPR2022-00761
Patent 7,498,633 B2

Before GRACE KARAFFA OBERMANN, JO-ANNE M. KOKOSKI,
and JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

OBERMANN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 325(d)

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I. INTRODUCTION

Petitioner filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 9–11 of U.S. Patent No. 7,498,633 B2 (Ex. 1001, “the ’633 patent”). Patent Owner filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). The Preliminary Response includes a request that the Board exercise its discretion to deny review under 35 U.S.C. § 325(d) (“Section 325(d)”). Prelim. Resp. 20–22. Petitioner filed a Reply (Paper 7, “Reply”) and Patent Owner filed a Sur-reply (Paper 8, “Sur-reply”), which address that request. Ex. 1024 (authorization). This Decision is based solely on the information presented in the Petition, Preliminary Response, Reply, and Sur-reply.

A. Real Parties-in-Interest

The Petition identifies “Wolfspeed” as the sole “real party-in-interest” for Petitioner. Pet. 5. Patent Owner’s Mandatory Notice identifies “The Trustees of Purdue University and the Purdue Research Foundation” as real parties-in-interest for Patent Owner. Paper 3, 1.

B. Related Matters

Both parties identify as a related matter the co-pending district court litigation in *The Trustees of Purdue University v. STMicroelectronics N.V. et al.*, No. 6:21-cv-00727 (W.D. Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-cv-840 (M.D.N.C.). Pet. 5; Paper 3, 1.

Both parties also identify a prior Board proceeding in IPR2022-00252 (“IPR252”). Pet. 5; Paper 3, 1. We issued a decision denying review in IPR252 on June 22, 2022. IPR252, Paper 13. Concurrently herewith, we issue a decision denying a request for rehearing in IPR252. Patent Owner,

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but not Petitioner, identifies IPR2022-00723 (“IPR723”). Pet. 5; Paper 3, 1. Concurrently herewith, we issue a decision denying review in IPR723.

II. BACKGROUND

A. The '633 Patent (Ex. 1001)

The '633 patent relates to a double-implanted metal-oxide semiconductor field effect transistor (“DIMOSFET”) having a substrate, drift layer, first source region, first source electrode, plurality of first base contact regions, second source region, second source electrode, plurality of second base contact regions, and junction field-effect transistor (“JFET”) region. Ex. 1001, 9:41–10:8.

According to the '633 patent, “[o]ne design consideration in the fabrication of” metal-oxide semiconductor field effect transistors (“MOSFETs”) “is the blocking voltage of the semiconductor device.” *Id.* at 1:18–21. The blocking voltage is “the drain-to-source voltage of the” MOSFET “at which avalanche breakdown occurs and/or the strength of the magnetic field of the gate oxide at which the gate oxide fails.” *Id.* at 1:21–25. For high-voltage power applications, a high blocking voltage generally is desirable. *Id.* at 1:25–27.

Another design consideration is “the specific on-resistance of the semiconductor device,” that is, “the product of the resistance of the device between the source and drain when the device is in an on-state and the area of the device.” *Id.* at 1:27–31. As the specific on-resistance decreases, efficiency of the semiconductor device may improve. *Id.* at 1:31–33. Typically, however, fabrication techniques that reduce the specific on-resistance of a high-voltage power MOSFET may also reduce the blocking voltage of the device. *Id.* at 1:33–36.

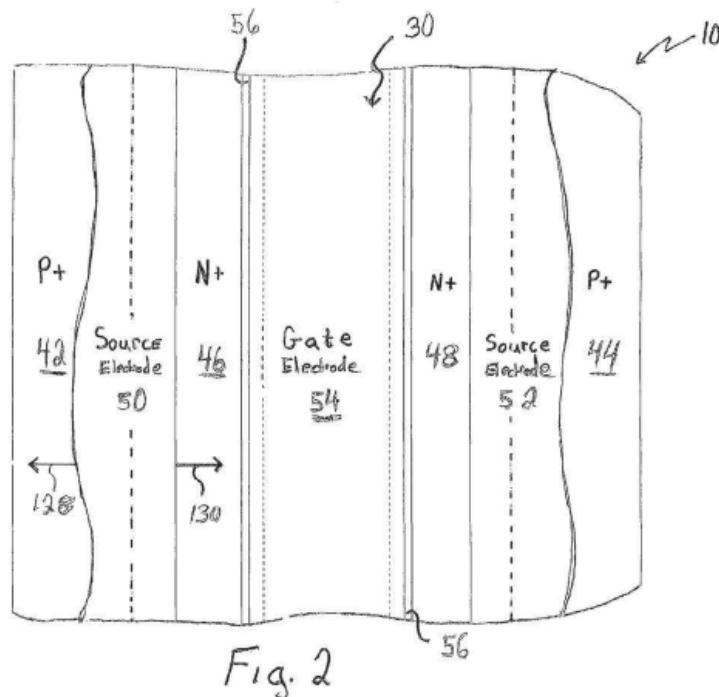
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The DIMOSFET of the claimed invention includes a “first source electrode formed over the first source region, the first source electrode defining a longitudinal axis” and “a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode.” *Id.* at 9:47–53 (claim 9). Similarly, the DIMOSFET includes a second source electrode formed over the first source region and a plurality of second base contact regions spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode. *Id.* at 9:55–10:5. The specified semiconductor device also includes a JFET region located between the first source region and the second source region and, in some embodiments, the JFET region has “a width less than about three micrometers.” *Id.* at 10:6–8 (claim 9). We next address advantages attributed to the claimed invention as described and illustrated in the ’633 patent.

The ’633 patent indicates that, at some point during the design process, “the specific on-resistance contribution of a JFET region of a MOSFET device is reduced to a point” where “the source resistance . . . becomes one of the dominating contributions to the specific on-resistance of the device.” *Id.* at 7:22–26. Manufacturing process variations, such as the topological configuration of Figure 2, reproduced below, may result in “an undesirable source resistance” if source regions 46 and 48 are misaligned with respect to base contact regions 42 and 44, or source regions 46 and 48 are misaligned with respect to source electrodes 50 and 52. *Id.* at 7:39–44.¹

¹ This disclosure misidentifies source region 52 as element 42. Compare Ex. 1001, 7:35–36 (correct numeric identifications), with *id.* at 7:44.

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Ex. 1001, Fig. 2. Figure 2 is a plan view of a portion of a semiconductor device of the claimed invention. *Id.* at 3:50–53. Figure 2 illustrates semiconductor device 10, including the locations of JFET region 30, gate electrode 54, source regions 46 and 48, which are doped with N-type (“n⁺”) impurities, base electrode regions 42 and 44, which are doped with P-type (“p⁺”) impurities, and source electrodes 50 and 52, which, respectively, are formed over source regions 46 and 48. *Id.* at 6:63–7:6.

“[T]he source regions 46, 48 and base contact regions 42, 44 extend longitudinally with and substantially parallel to the source electrodes 50, 52 and the JFET region 30.” *Id.* at 7:35–38. The '633 patent explains:

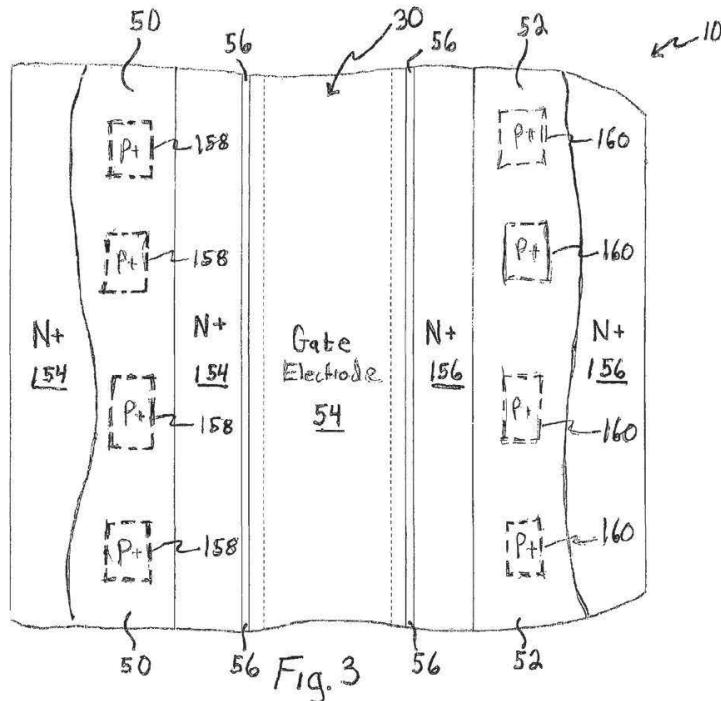
Because of semiconductor manufacturing process variations, such a topological configuration as illustrated in FIG. 2 can result in an undesirable source resistance if the source regions 46, 48 are misaligned with respect to the base contact regions 42, 44 and/or the source regions 46, 48 are misaligned with respect to the source electrodes 50, [5]2. For example, with

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respect to the source region 46, if the source electrode 50 is inadvertently formed more toward the direction of arrow 128 and/or the source region 46 is inadvertently formed more toward the direction of arrow 130, the source electrode 50 may not adequately cover the source region 46 and thereby cause the source resistance of the semiconductor device 10 to be increased due to the misalignment.

Id. at 7:39–51.

“[T]o reduce the likelihood of misalignment between the source electrodes and the source regions,” the semiconductor device of the claimed invention “is fabricated to have source regions” that each include a plurality of base contact regions, formed in the base source regions, respectively. *Id.* at 7:52–57. For example, the base contact regions may be “embodied as small ‘islands’ or regions within the larger source regions.” *Id.* at 7:57–59. Such a configuration is illustrated in Figure 3, which we reproduce below.



Ex. 1001, Fig. 3. Figure 3 is a plan view of an embodiment of the invention of the '633 patent. *Id.* 3:54–55. Figure 3 illustrates semiconductor device 10,

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which includes base contact regions 158 and 160 that are “embodied as small ‘islands’ or regions within the larger source regions” denoted as elements 154 and 156. *Id.* at 7:57–59. “The base contact regions 158, 160 are formed to be located in a central location under the source metallic electrodes 50, 52 with areas of source regions 154, 156” that are “spaced between each base contact region[.]” *Id.* at 7:59–63. “Because the source regions 154, 156 form a greater portion of the area under the source electrodes 50, 52, the tolerance to manufacturing variability of the semiconductor device 10 may be increased.” *Id.* at 7:65–8:1. Thus, “even if the source electrodes 50, 52 are slightly misaligned with respect to the source regions 154, 156, the source resistance of the semiconductor device 10 is not substantially increased,” given that “a substantial portion of the source regions 154, 156 would remain aligned with the respective source electrode 50, 52.” *Id.* at 8:1–6.

The ’633 patent explains other advantages associated with the claimed invention by reference to Figure 1, which we reproduce below.

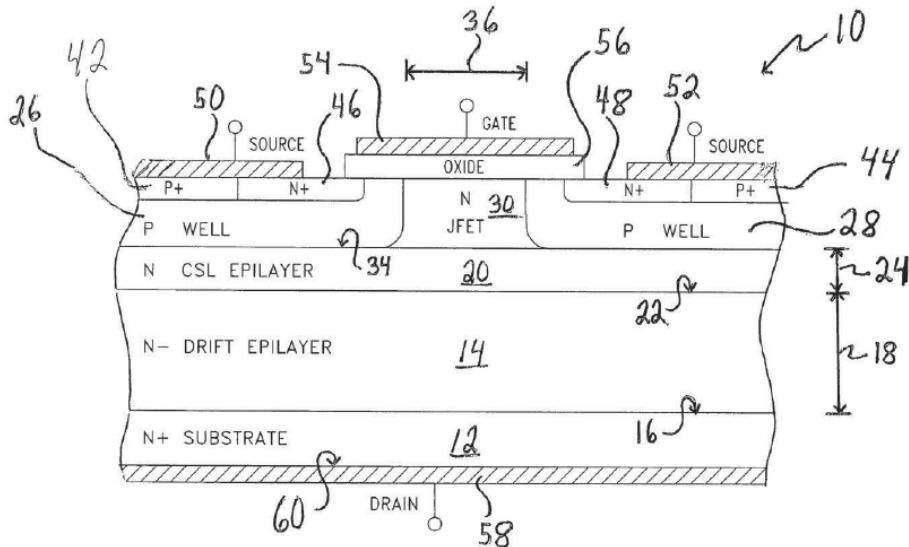


Fig. 1

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Ex. 1001, Fig. 1. Figure 1 is a diagrammatic cross-sectional view of an embodiment of semiconductor device 10. According to the '633 patent, JFET region 30 may be “fabricated to have a short width 36 relative to a typical DMOSFET device, which may reduce the specific on-resistance of the semiconductor device 10.” *Id.* at 6:21–24. For example, in some embodiments, “JFET region 30 has a width 36 that is about three micrometers or less.” *Id.* at 6:24–26 (referring to Figure 1).

B. Challenged Claims

We reproduce below independent claim 9.

9. A double-implanted metal-oxide semiconductor field-effect transistor comprising:

- a silicon-carbide substrate;
- a drift semiconductor layer formed on a front side of the semiconductor substrate;
- a first source region;
- a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
- a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
- a second source region;
- a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
- a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
- a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

Ex. 1001, 9:41–10:8.

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Claims 10 and 11 depend from claim 9 and impose additional limitations on the JFET region. *Id.* at 10:9–18. Specifically, claim 10 specifies that “the JFET region has a width of about one micrometer.” *Id.* at 10:9–11. Claim 11, by contrast, imposes limitations pertaining to the relative concentrations of “first type impurities” included in the JFET region and drift semiconductor layer. *Id.* at 11:12–18.

C. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 9–11 on two grounds:

Ground	35 U.S.C. §	Reference(s)
1	103 ²	Ryu ³ and Depetro ⁴
2	103	Ryu and Choy ⁵

Pet. 2. Petitioner relies on the Declaration of Jack Lee, Ph.D. (Ex. 1010).

III. ANALYSIS

A. Level of Ordinary Skill in the Art

The level of ordinary skill in the art at the time of the invention is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)).

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the ’633 patent has an effective filing date before March 16, 2013 (Ex. 1001, codes (22), (60), (65)), we refer to the pre-AIA version of Section 103.

³ U.S. Patent Application Publication No. 2004/0119076 A1, published June 24, 2004, filed October 30, 2003 (Ex. 1003).

⁴ U.S. Patent No. 6,043,532, issued March 28, 2000 (Ex. 1004).

⁵ U.S. Patent No. 5,171,705, issued Dec. 15, 1992 (Ex. 1005).

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In this Decision, we assess the asserted obviousness grounds only to the extent necessary to resolve Patent Owner’s request that we exercise our discretion and deny the Petition under Section 325(d).

The parties disagree about the level of ordinary skill in the art at the time of the invention. *Compare* Pet. 29 (Petitioner’s asserted definition of the ordinarily skilled artisan), *with* Prelim. Resp. 15–18 (opposing Petitioner’s definition and proposing an alternative definition). We decline to resolve that dispute because, on this record, neither party demonstrates that the selection of one definition over the other would change the ultimate result under Section 325(d). Based on the information presented, we find that the asserted prior art itself is sufficient to demonstrate the level of skill in the art at the time of the invention for the purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself can reflect the appropriate level of ordinary skill in the art).

B. Claim Construction

We construe claim terms only as relevant to the parties’ contentions and only to the extent necessary to resolve the issues in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). No claim term requires express construction in order to resolve whether we should exercise our discretion and deny the Petition under Section 325(d).

C. Discretionary Denial Pursuant to Section 325(d)

The Board may institute an *inter partes* review where the information presented “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least [one] of the claims challenged in the

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petition.” 35 U.S.C. § 314(a). Even where a petitioner meets that threshold showing, however, the Board has discretion to deny the request for review where the petitioner advances “the same or substantially the same prior art or arguments previously” presented to the Office. 35 U.S.C. § 325(d).

Petitioner does not contest Patent Owner’s view that the discretionary denial provisions of Section 325(d) apply in cases where the information presented shows that “substantially the same prior art” previously was presented to the Board in an earlier-filed petition for *inter partes* review. 35 U.S.C. § 325(d); *compare* Prelim. Resp. 20 (Patent Owner’s argument, including citations to supporting cases), *with* Reply 1–3 (nowhere contesting that argument). Accordingly, in this section of our analysis, we resolve whether a discretionary denial is warranted in this proceeding based on the petition filed in IPR252. *See* Ex. 2027 (earlier-filed petition for *inter partes* review challenging the same patent claims at issue in the instant case).

We apply a two-part framework when assessing whether to exercise our discretion to deny a petition under Section 325(d). First, we consider whether the same or substantially the same prior art or arguments previously were presented to the Office. Second, if either condition is satisfied, we assess whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) (setting forth two-part framework that guides the Board’s decision whether to exercise its discretion to deny review under Section 325(d)). In this Decision, we limit our discussion to whether Petitioner (1) advances substantially the same

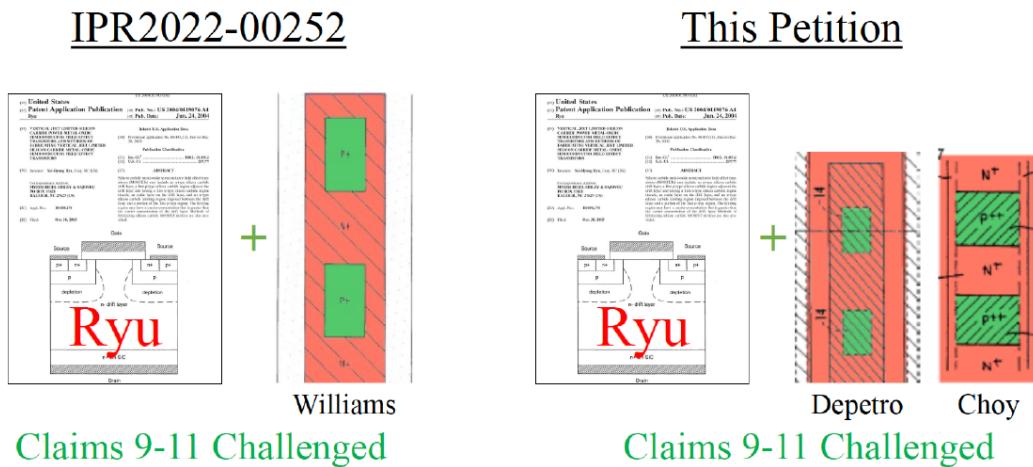
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prior art⁶ previously presented in IPR252; and (2) demonstrates a material error in the Board’s decision denying institution of review in IPR252.

1. Substantially the Same Prior Art as in IPR252

The Petition in IPR252 asserts a single ground of unpatentability against the challenged claims based on obviousness over Ryu and Williams⁷. Ex. 2027, 4. The instant Petition, by contrast, asserts two obviousness grounds—one based on Ryu and Depetro and another based on Ryu and Choy. Pet. 7. As an initial matter, we find that the same prior art reference, Ryu, is applied in both the instant Petition and the IPR252 petition.

A question arises whether Depetro and Choy are substantially the same prior art as Williams. On that point, Patent Owner directs us to the following illustration:



Prelim. Resp. 21. The above illustration compares Ryu and Williams as advanced in IPR252 (on the left) and Ryu, Depetro, and Choy as advanced

⁶ The connector “or” in Section 325(d) renders moot whether the Petition raises substantially the same arguments presented in IPR252. *See* Sur-reply 3 (“denial is warranted based on ‘substantially the same prior art **or** arguments’”) (quoting Section 325(d)) (Patent Owner’s emphasis).

⁷ U.S. Patent No. 6,413,822 B2, issued July 2, 2002 (Ex. 1006).

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in the instant Petition (on the right). The illustration shows that both Depetro and Choy disclose the same formation of p+ regions, as windows in an n+ source region, as disclosed in Williams—and this source-region layout is the claimed feature that Petitioner asserts is missing in Ryu’s MOSFET. *Id.*

As Patent Owner observes, Petitioner, in the Petition, “admits ‘Williams . . . teaches the same source-regions layout as Depetro’ and ‘Choy.’” Prelim. Resp. 21–22 (quoting Pet. 65, 90). In the Reply, however, Petitioner retreats from that admission, asserting that the Petition “presents materially different prior art” than the petition in IPR252. Reply 1–2. By way of support, Petitioner argues that Depetro, unlike Williams, discloses a “strongly doped p+ region” and, further, that Choy, unlike Williams, discloses “self-aligned p++ regions.” Reply 1–2 & n.1. Petitioner does not explain sufficiently, if at all, how those asserted differences are material to the challenges at hand. *Id.* at 2–3 & n.1.

Patent Owner, by contrast, explains why those differences are immaterial to the challenges at hand. Specifically, as Patent Owner points out, the “strongly doped p+ region” advanced by Petitioner in the Reply is disclosed in Depetro’s Figure 5, but “the Petition consistently” advances “Depetro’s Figure 1 source-region layout, *without* a strongly doped p+ region,” as the disclosure that is “applied to the DIMOSFET of Ryu.” Sur-reply 2 (Patent Owner’s emphasis); *see* Pet. 3, 40, 42, 47–49, 51–52, 57–58, 64–65 (supporting examples from the instant Petition).

Similarly, as to Choy’s “self-aligned p++ regions,” Patent Owner points out that Petitioner does *not* rely on that feature in the ground that asserts Choy. *See* Sur-reply 2 (the Reply “cites Choy’s alleged ‘self-aligned p++ regions,’” but “the Petition never submits that teaching”). Petitioner, in

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the Petition, relies on Choy’s “source-regions layout” and emphasizes that Williams discloses that “same” feature, and, further, in the Reply, provides no contrary analysis. Reply 2 n.1; *cf.* Pet. 90 (ground based on Choy, asserting that Williams “teaches the same source-regions layout as Choy,” in which “p+ contacts” are “formed as spaced-apart regions in the n+ source region”).

In Patent Owner’s view, Petitioner advances “new assertions” in the Reply that are designed “to gloss over the fact” that the Petition advances substantially the same prior art asserted in IPR252.⁸ Sur-reply 2–3. We agree only that the disclosures of Depetro and Choy, as advanced in the Petition, are substantially the same as those reflected in Williams. Prelim. Resp. 21 (Patent Owner’s illustration, reproduced *supra* 12, comparing relevant disclosures of Ryu, Williams, Depetro, and Choy). We agree with Patent Owner that this is supported by Petitioner’s own assertions, as set forth in the Petition, acknowledging that Depetro and Choy disclose the “same base contact designs” as Williams. Prelim. Resp. 21–22 (citing Pet. 65, 90). Williams is substantially similar to Depetro and Choy and, thus, the first prong of *Advanced Bionics* is met.

2. Material Error in the Institution Decision in IPR252

Petitioner does not address whether the Board materially erred in its decision denying institution in IPR252. *See* Pet. 97; Reply 2–3. In the Petition, Petitioner does not address the applicability of Section 325(d) to IPR252. *See* Pet. 97. In the Reply, Petitioner addresses Section 325(d), as

⁸ Notably, the Board’s decision denying institution in IPR252 issued *after* the filing of the Petition but *before* the filing of Petitioner’s Reply.

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applicable to IPR252, but stops short of identifying any error, much less a material error, in the prior decision. Reply 2–3.

On this record, Petitioner has not “demonstrated that the Office erred in a manner material to the patentability of the challenged claims” in IPR252. *Advanced Bionics*, Paper 6 at 8. As Patent Owner points out, “Petitioner does not even dispute the second prong of *Advanced Bionics*.” Sur-reply 1 (citing Prelim. Resp. 22; Reply 3).

IV. CONCLUSION

Petitioner raises substantially the same prior art previously presented to the Board in IPR252. Petitioner does not demonstrate that the Board erred in a manner material to the patentability of the challenged claims in the decision denying institution in IPR252. Taking a holistic view of the totality of the circumstances presented, on this record, we exercise our discretion under Section 325(d) and do not institute an *inter partes* review.

V. ORDER

It is
ORDERED that the Petition is *denied* and no *inter partes* review is instituted.

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